

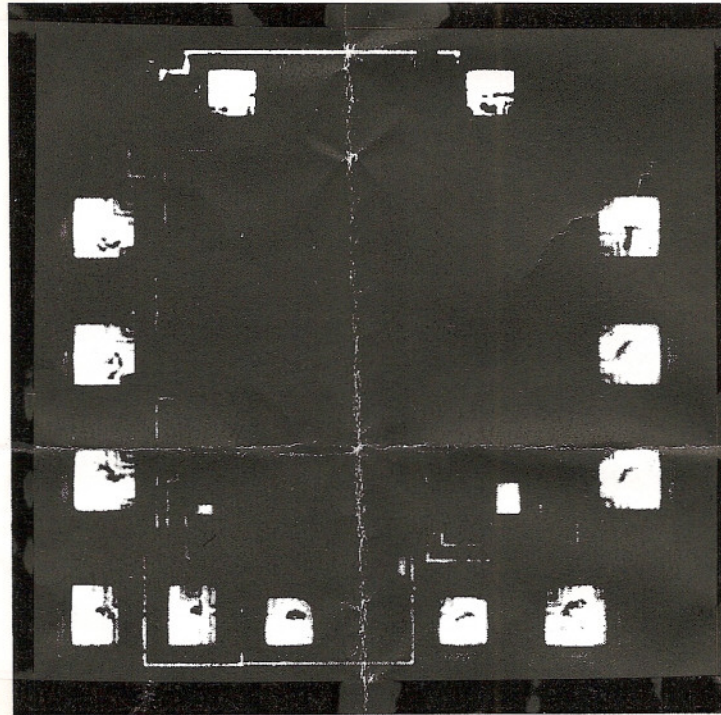


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal:**  
**Backside:**  
**Backside Potential:**  
**Mask Ref:**  
**Bond Pads (Mils):**

**APPROVED BY:**  
**MFG: NSC (CL)**

**DIE SIZE (Mils): 55 x 55**  
**THICKNESS:**

**DATE: 12/23/99**  
**P/N: CLC520ALC**